Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.026”**



**.026”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004” min.**

**Backside Potential: Collector**

**Mask Ref: CP710**

**APPROVED BY: DK DIE SIZE .026” X .026” DATE: 5/23/16**

**MFG: CENTRAL SEMI THICKNESS .009” P/N: CMPTA94**

**DG 10.1.2**

#### Rev B, 7/19/02